IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

1. (previously presented) A nonvolatile memory apparatus comprising:

a control circuit;

a plurality of terminals including a clock terminal, a command terminal and other terminal;

a clock generator;

a data buffer;

a command buffer; and

a plurality of nonvolatile memory cells,

wherein said clock terminal receives a first clock signal,

wherein said clock generator is controlled by said control circuit for generating a second clock signal,

wherein said command terminal couples to said command buffer and receives commands which comprise a read command and a program command,

wherein said data buffer is used for receiving data from outside and outputting data to outside,

wherein said control circuit reads out operation steps from a program memory for controlling an operation of said received command by executing said operation steps,

wherein in an operation in response to said read command, said control circuit controls, based on operation steps corresponding to said read

command, reading data from ones of said nonvolatile memory cells, stores read data to said data buffer, and outputting said read data stored in said data buffer via said other terminal except said command terminal in response to said clock signal,

wherein in an operation in response to said program command received from said command terminal, said control circuit controls, based on operation steps corresponding to said program command, receiving data via said other terminal except said command terminal in response to clock signal, stores received data to said data buffer and writing said received data to ones of said nonvolatile memory cells, and

wherein said data writing to ones of said nonvolatile memory cells is performed using said second clock signal.

2. (original) A nonvolatile memory apparatus according to claim 1, further comprising;

a decode circuit,

wherein said decode circuit decodes said commands received in said command buffer.

3. (original) A nonvolatile memory apparatus according to claim 2, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range Indicating said program state and staying threshold voltages of remaining memory cells of ones of said nonvolatile memory cells within said threshold voltage range indicating said erase state, based on said operation steps corresponding to said program command.

4. (original) A nonvolatile memory apparatus according to claim 3, wherein said command further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said control circuit controls moving said threshold voltages of ones of said nonvolatile memory cells to within said threshold voltage range indicating said erase state, based on said operation steps corresponding to said erase command.

5. (original) A nonvolatile memory apparatus according to claim 4, wherein said control circuit comprises a circuit, and

wherein in said operation in response to read command, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

6. (original) A nonvolatile memory apparatus according to claim 5, wherein said other terminal is a data terminal,

wherein in said operation in response to said program command, said data terminal receives data in response to said clock signal, and

wherein in said operation in response to said read command, said data terminal outputs data in response to said clock signal.

7. (original) A nonvolatile memory apparatus according to claim 1, wherein said control circuit includes said program memory therein.

8. (original) A nonvolatile memory apparatus according to claim 2, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each indicating a corresponding program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltages indicating said program states according to data and staying said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells, based on said operation steps corresponding to said program command.

9. (original) A nonvolatile memory apparatus according to claim 8, wherein said command further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said control circuit controls moving said threshold voltages of ones of nonvolatile memory cells to within said threshold voltage range indicating said erase state, based on said operation steps corresponding to said erase command.

10. (previously presented) A nonvolatile memory apparatus comprising:

a control circuit;

a first volatile memory;

a second volatile memory;

a clock terminal;

a data terminal:

a command terminal;

a clock generator; and

a plurality of nonvolatile memory cells,

wherein said clock terminal receives a first clock signal,

wherein said clock generator is controlled by said control circuit for generating a second clock signal,

wherein said data terminal couples to said first volatile memory,

wherein said command terminal couples to said second volatile memory receives commands which include a read command and a program command,

wherein said control circuit executes operation steps corresponding to a received command read out from a program memory,

wherein in an operation in response to said read command received from said command terminal, said control circuit controls, based on operation steps corresponding to said read command, reading data from ones of said nonvolatile memory cells, transferring read data to said first volatile memory, and serially outputting said read data from said first volatile memory via said data terminal in response to said clock signal,

wherein in an operation in response to said program command received from said command terminal, said control circuit controls, based on operation steps, corresponding to said program command, serially receiving of data via said data terminal in response to said clock signal, transferring received data to said first volatile memory, and writing said received data stored in said first volatile memory to ones of said nonvolatile memory cells, and

wherein said data writing to ones of said nonvolatile memory cells is performed using said second clock signal.

11. (original) A nonvolatile memory apparatus according to claim 10, further comprising:

a decode circuit,

wherein said decode circuit decodes said commands received in said second volatile memory.

12. (original) A nonvolatile memory apparatus according to claim 11, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a threshold voltage range indicating a program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within said threshold voltage range indicating said program state and staying threshold voltages of remaining memory cells of ones of said nonvolatile memory cells within said threshold voltage range indicating said erase state, based on said operation steps corresponding to said program command.

13. (original) A nonvolatile memory apparatus according to claim 12, wherein said command further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said control circuit controls moving said threshold voltage of ones of nonvolatile memory cells to within said threshold voltage range

indicating said erase state, based on said operation steps corresponding to said erase command.

14. (original) A nonvolatile memory apparatus according to claim 13, wherein said control circuit comprises a circuit, and

wherein in said operation in response to read command, said circuit senses status of data according to threshold voltage of said nonvolatile memory cell which is within whether said threshold voltage range indicating said erase state or said threshold voltage range indicating said program state.

15. (original) A nonvolatile memory apparatus according to claim 10, wherein said control circuit includes said program memory therein.

16. (original) A nonvolatile memory apparatus according to claim 11, wherein each of said nonvolatile memory cells has a threshold voltage within an arbitrary one of a plurality of threshold voltage ranges,

wherein said threshold voltage ranges comprise a threshold voltage range indicating an erase state and a plurality of threshold voltage ranges each of indicating a corresponding program state, and

wherein said nonvolatile memory apparatus controls moving said threshold voltage of one nonvolatile memory cell to within one of said threshold voltage ranges indicating said program states according to data and staying said threshold voltages of remaining memory cells of ones of said nonvolatile memory cells, based on said operation steps corresponding to said program command.

17. (original) A nonvolatile memory apparatus according to claim 16, wherein said command further comprises:

an erase command,

wherein in an operation in response to said erase command received from said command terminal, said control circuit controls, based on operation steps corresponding to said erase command, erasing of data stored in ones of said nonvolatile memory cells, and

wherein said control circuit controls moving said threshold voltages of ones of nonvolatile memory cells to within said threshold voltage range indicating said erase state, based on said operation steps corresponding to said erase command.

18. (new) A nonvolatile memory apparatus comprising:

a nonvolatile memory part including a plurality of nonvolatile memory cells and a first buffer;

a control part having a program memory;

a second buffer;

a clock generator; and

a plurality of terminals including a clock terminal, a command terminal and a data terminal,

wherein said clock terminal is capable of receiving a first clock signal,

wherein said command terminal is capable of receiving commands which include a read command and a program command,

wherein said clock generator is capable of generating a second clock which is provided to said nonvolatile memory part,

wherein said program memory is accessed in response to receiving command,

wherein in an operation in response to said read command received from said command terminal, said control part makes ones of said nonvolatile memory cells in said nonvolatile memory part read out data to said first buffer, transfer data from said first buffer to said second buffer, and then outputs data stored in said second buffer via said data terminal in response to said first clock signal, and

wherein in an operation in response to said program command received from said command terminal, said control part receives data via said data terminal in response to said first clock signal to said second buffer, transfers data from said second buffer to said first buffer, and then makes ones of said nonvolatile memory cells in said nonvolatile memory part store data using said second clock signal.

19. (new) A nonvolatile memory apparatus according to claim 9, wherein said command further include an erase command, and

wherein in an operation in response to said erase command received from said command terminal, said control part makes ones of said nonvolatile memory cells in said nonvolatile memory part erase data stored therein.

20. (new) A nonvolatile memory apparatus according to claim 10,

wherein said control part includes a command decoder, which is used for deciding operation in accordance with received command via said command terminal.

21. (new) A nonvolatile memory apparatus according to claim 11, wherein said control part further includes a sequencer which accesses to said program memory in accordance with said received command.